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Methodologies for high-speed and low-power VLSI design

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ABSTRACT

High-Speed and Low-power are the major challenges for today's electronics industries. Power dissipation is an important consideration in terms of Speed/Performance and space for VLSI Chip design. Power management techniques are generally used to designing low power circuits and systems. This thesis presents the various VLSI Design Methodologies for high Speed and Low power management techniques that can meet future challenges to designs low power high speed/performance circuits, algorithm level design. It also describes the many issues regarding circuits design at architectural, logic and device levels and presents various techniques to overcome difficulties.

Keywords: *VLSI, High Speed, Low Power consumption, MHS-Domino gates, CMOS, Clock gating etc.*

1. INTRODUCTION

Since the invention of the first Integrated Circuit (IC) three decades ago, designers have been looking for methods to Speed up digital circuits and to reduce the Power and Area of their designs. Recently, advances in VLSI fabrication technology have made it possible to put a complete System on a Chip (SOC) which facilitates the development of Personal Digital Assistances (PDA's), cellular phones, laptops, hand-held computers, and mobiles multimedia systems. The evolution of these applications profiles power dissipation as a critical parameter in digital VLSI design.

The Speed/performance continues to be the main target for digital designers. Consumers expect higher speed, more functionality, and higher levels of integration, from their cellular phones and hand-helds. To emphasize the importance of speed, researchers use Energy Delay Product (EDP) as an evolution figure for digital systems. Consequently, reducing power dissipation should not come at the expense of performance. In the meantime, increasing Speed while keeping power dissipation constant is also considered to be a low-power design problem.

Power dissipation is defined as the rate of energy delivered from the source to the system/device. In battery operated systems, the amount of energy stored in the battery is limited. Therefore, power dissipation is important for portable systems, as it defines the average lifetime of the battery. Unfortunately, battery Technology is not expected to improve the battery storage capacity by more than 30% every five years. This is not sufficient to handle the increasing power requirements of portable systems. Low- power devices are expected to have smaller battery size, less weight, and longer battery lifetime.

The objective of this dissertation is to develop Low-power VLSI Design methodologies to reduce power and enhance speed/performance simultaneously. The thesis covers low-power design on different design stages, beginning from the process level up to the algorithms level. On the process level, the impact of CMOS technology scaling on power, delay, and area of various logic styles is presented along with predictions for future scalability of each logic style. On the circuit level, two new circuit techniques to enhance performance and reduce power dissipation are presented. On the algorithm level, a low-power algorithm for high radix division is proposed.

By increasing the speed and reducing the power, area of digital systems we are focusing on VLSI Design Methodologies. However, the evolution of portable systems and advanced Deep Sub-Micron (DSM) fabrication technologies has brought power dissipation as another critical design factor. Low-power design reduces cooling cost and increases reliability especially for high-density systems. Moreover, it reduces the weight and size of portable devices. Yes, high-performance is still the main criterion for most digital systems, which may not be sacrificed to achieve lower power dissipation. This thesis presents new low-power high-performance digital VLSI design methodologies for process, circuit, and algorithm level design.

On the process level, future challenges in device scaling such as short channel effects, sub threshold leakage currents, and hot carrier effects are discussed. The influence of technology scaling on the performance, power, and area of different CMOS logic styles is then analyzed and simulated. This study covers five logic families, namely COMS, CPL, Domino, DCVS, and CML. The scalability of each logic style and its potential in future technology generation are explored. On the circuit level, a new logic family for low-power high-performance applications is presented. This logic family combines the speed, low supply voltage, and noise immunity of CML circuits with the low standby current and design simplicity of dynamic circuit. The new logic style reduces the power by 70% and the delay by 73% compared to conventional CMOS logic. A 16-bit CLA adder is designed, simulated, fabricated, and tested using 0.6µm COMS technology. Test results have confirmed the functionality of the new logic family at various supply voltages.

Also, a new Domino logic style, called High-Speed Domino (HS-Domino), has been developed. Hs-Domino resolves the trade-off between noise margin and speed associated with the conventional Domino logic. Simulation results show that HS-Domino circuit is superior to conventional Domino once in terms of power, speed, and tolerance to the leakage currents in DSM technologies.

This thesis also presents new Multiple Threshold CMOS (MTCMOS) scheme for dynamic circuits. This scheme is applied to Domino and DDCVS logic styles. The new implementations reduce the leakage power by orders of magnitude keeping the noise margin intact and maintain the high Speed/performance and low dynamic power of low VT circuits. Unlike other MTCMOS Domino logic implementations, the new scheme does not require additional hardware. At the algorithm level, a new algorithm for high radix division is presented. The algorithm uses a look-up table to estimate the quotient digit at each iteration. The look-up table is optimized to reduce power dissipation and delay of the divider. Simulation results show that the new algorithm reduces the power dissipation by 22% and 12% for radix 8 and radix 16 divisions, respectively, compared to other division algorithms. The algorithm also increases the speed by a factor of 13% and 10% for radix 8 and radix 16 divisions, respectively.

2. LOW-POWER VLSI METHODOLOGIES

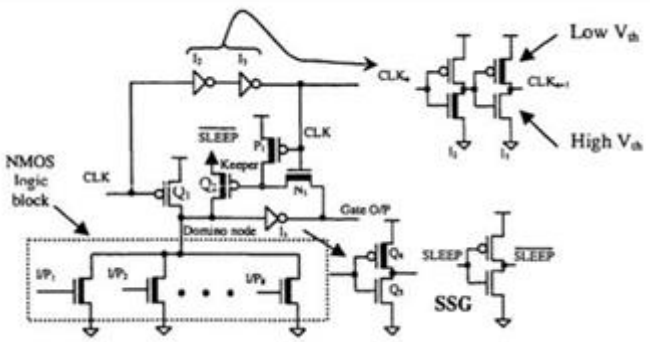
In order to increase the speed and reduce the Power dissipation, many modifications may be applied to the process. These modifications include reducing the threshold voltage, reducing minimum gate length, and increasing the number of metal layers. Power dissipation may also be reduced by using alternative fabrication technology other than the CMOS process.

- Threshold Voltage Reduction
- Technology Scaling
- Increasing Number of Metal Layers
- Alternative Technologies

a) Silicon on Insulator (SOI)
b) Multi-Threshold Voltage (MTCMOS) Device
c) Low-Temperature CMOS (LTCMOS)
d) Dynamic Substrate Biasing
e) New Gate Oxide Materials

3. MTCMOS HIGH-SPEED DOMINO LOGIC (MHS-DOMINO)

To resolve the speed-NM trade-off, and thus remove the contention, as well as achieving ultra-low leakage values, the MTCMOS HS-Domino (MHS-Domino) circuit shown in below.



An 8-input MHS-Domino OR Gate

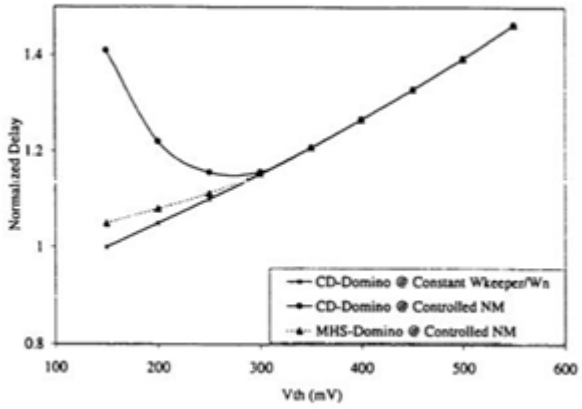
The MHS-Domino gate is similar to the HS-Domino gate, except that the keeper source is connected to SLEEP (SSG-out) signal instead of VDD. Transistors of the NMOS logic block, Q2, Q4, P1, N1, the NMOS transistor of I2, and the PCOM transistor of I3 are LVT transistors to speed up evaluation. The MHS-Domino circuit employs a Sleep Signal Generator (SSG), which is realized by a simple inverter as shown in the schematic. The PMOC device of the SSG must be kept HVT in order to reduce the leakage during standby. The SLEEP (SSG-in) signal is "0" for normal operation and "1" for standby.

During normal operation, the operation of MHS-Domino gate is the same as HS-Domino. In this mode, SLEEP (SSG-out) signal is "1". Therefore, the keeper source is connected to VDD through the SSG block. In this scheme, all the transistors involved during evaluation are LVT devices to reduce delay.

In standby mode, the SLEEP (SSG-in) signal is "1", SLEEP (SSG-out) becomes "0", and the clock is high. The Domino node has two possible outputs, "1" or "0". When the domino node is "0", the gate output is "1". Therefore the input to the following gate is "1". When the Domino node is "1", the output is "0" which turns the keeper transistor ON discharging the Domino node to SLEEP (SSG-out) signal and causing the gate output to turn into "1". This transition is fast because the keeper transistor is LVT. Therefore, at the beginning of standby operation, all MHS-Domino gates change their output to become "1" without using input gating which reduces hardware and power. After the initial transitions, transistors Q1, Q4, the NMOS of I2, the PMOS I3, and the PMOS of the SSG turn OFF. All these transistors have HVT to reduce the leakage current.

4. SPEED COMPARISION

The Speed advantage of MHS-Domino circuit, the normalized delay of a 3-stage chain of an 8-input Domino OR gates with a fan-out of 3 for the new MHS-Domino circuit versus Vth is shown as the 3rd curve in below figure. The delay curves of the MTCOMS Domino with constant NM and Content W (keeper)/Wn ratio are plotted on the same graph to illustrate the speed advantage of the MHS-Domino circuit. The below figure shows the delay of the MTCMOS modified circuit at constant NM continues to decrease as Vth is scaled down because there is no contention current.



Normalized delay of DVT Domino versus Vth

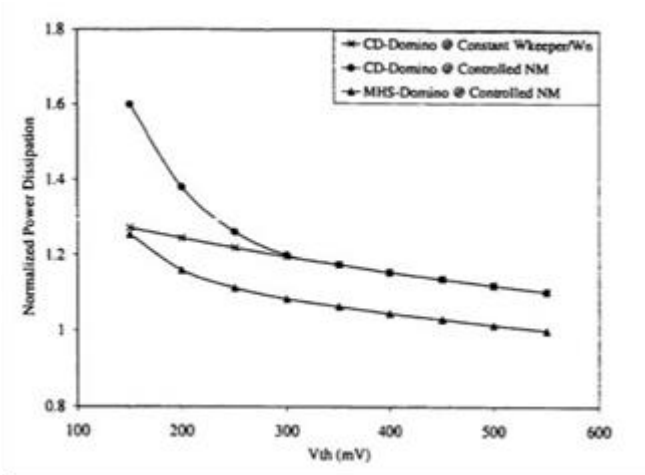
5. DYNAMIC POWER COMPARISON

The below figure shows the compares the MHS-Domino circuit with the MTCMOS CD-Domino circuit in terms of dynamic power.

Although the MHS-Domino circuit introduces slightly higher loading, and an SSG, it actually has significantly lower power dissipation than the conventional version. This is attributed to the following:

1) Eliminating of the contention in the modified Domino gate, this means that there are no short-circuit currents during switching.

2) N1 and P1 are minimum sized devices, contributed to a very small loading effect.



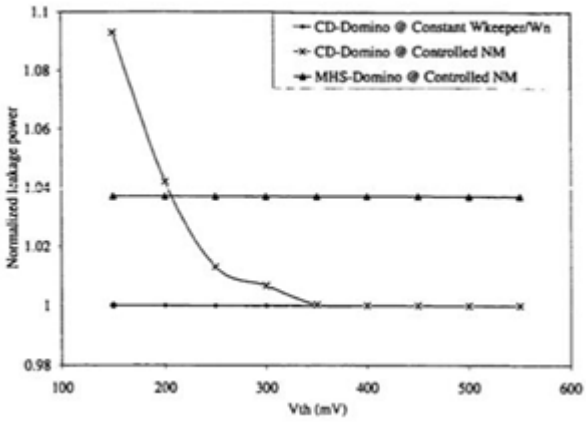
Normalized dynamic power in MTCMOS Domino versus Vth

3) The sleep signal generator hardly consumes any dynamic power because its output is always "1" during the active mode and "0 during standby.

Thus, no switching occurs except during transition from one mode to the other. These transitions are not frequent and its power dissipation is negligible.

6. LEAKAGE COMPARISON

A comparison between the normalized leakage power of the MTCMOS CD-Domino and MHS-Domino is shown in below figure. The leakage curves are plotted versus Vth for the MTCMOS Domino gate for constant NM and constant W(keeper)/Wn ratio (NM is ignored).



Normalized leakage power in MTCMOS Domino versus Vth

MHS-Domino consumes only 4% more leakage power than the MTCMOS CD-Domino (ignoring NM), while it also consumes slightly more leakage than the conventional MTCMOS case at constant NM until a Vth of ≈ 220mV. For Vth below 220mV, the MHS-Domino at constant NM has a leakage advantage over the conventional version at constant NM. It is necessary to offset the power penalty paid in turning devices ON and OFF, especially due to switching the devices from standby to active status, and vice versa. This power penalty becomes less significant if the system spends most of its time in the idle state (95%).

Therefore, MHS-Domino eliminates the contention, enhances the speed/performance, reduces power dissipation and reduces leakage current during standby.

The scheme used to convert HS-Domino to an MTCMOS logic style is generic and is applied to any other dynamic logic style.

7. CONCLUSION AND FUTURE SCOPE

In this paper, various strategies and methodologies for High speed and power consumptions are discussed and review. The need for lower power systems is being driven by many market segments. Unfortunately designing for low power adds another dimension to the already complex design problem and the design has to be optimized for power as well as speed/Performance and Area. Energy consumption breaks down into dynamic, static, leakage and short circuit power dissipation. Dynamic power, with a share of 80% is the starting-point for most of the introduced methodologies. A low voltage/low threshold technology and circuit design approach, targeting supply voltages around 1 Volt and operating with reduced thresholds.

Conclusion

Design for High-speed/performance and Low-power has become an important concern in VLSI design, especially for portable systems where the energy source, the battery, is limited. The reduction of the transistor size allows higher integration density and increases the operating frequency. This work introduced a new methodology for High-speed and Low Power digital design, on the process, circuit and algorithm levels.

Future Work

Engineers expected that the dynamic logic styles not to be attractive in VLSI technologies. This thesis introduced new circuit techniques. Further enhancements to this work should include developing more accurate models for leakage currents and implement those circuits on real silicon to validate their functionality when such technologies become available.

This scheme is extended to Domino Dual Cascade Voltage Switch Logic (DDCVS).

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