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Analysis and Performance Evaluation of Nano-Scale Semiconductor Devices

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ABSTRACT

The current work in this paper deals with the analysis and comparison of single gate silicon on insulator (SG-SOI) MOSFET and double gate silicon on insulator (DG-SOI) MOSFET. Both the devices have 20nm Fin width and a channel length of 50nm. The quantitative analysis of these nanoscale gate devices and comparison between their parameters such as Subthreshold Slope (SS), the Threshold voltage (V_t), transconductance(g_m), output conductance(g_d). This resulted in a reduction of short channel effects (SCE's) in the double gate MOSFET. The simulation of both the devices is done using ATLAS Simulator is SILVACO TCAD.

Keyword: *Silvaco Tcad, DG-SOI, SG-SOI.*

1. INTRODUCTION

The basic idea and motivation behind the advancement of CMOS technology for making the digital circuits are to decrease the price and to increase the performance hand to hand. The law which persistivity represent the evolution of CMOS technology is Moore's Law. It is the concise illustration of continuously increasing in the evolution of miniaturization. The devices and circuits are successfully achieved to work on 10nm scaling. The main challenge faced while miniaturization, is the submerged leakage current, short channel effects (SCE's) etc. To minimize all these effects, an ultra-narrowed structure is required. The work of this project consists of the device structure, simulation, result and discussion.

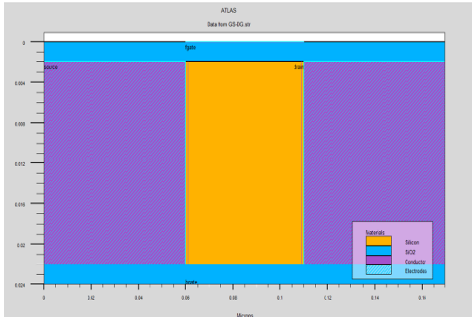


Fig 1(a.): Double Gate Simulated Structure

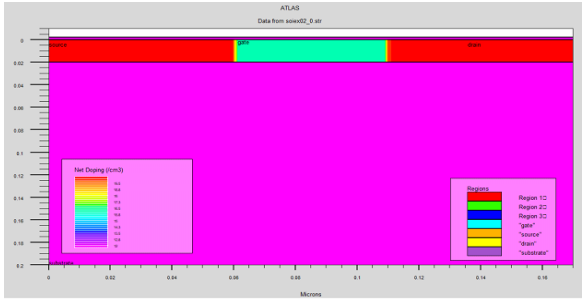


Fig 1(b): Single Gate Simulated Structure

Device Structure

Fig 1a-1b shows the representation of the simulated cross section in 2D. In this structure, dimensions are shown as:

PHYSICAL PARAMETERS	VALUE
Channel length	50nm
Source and drain length(L_s,L_d)	60nm
Gate oxide thickness	2nm
Channel doping	1e16

Source and drain doping	1e20
Metal gate work function	4.6ev

2. SIMULATION PROCEDURE

The parameters which we have used and the voltage which is supplied to the device simulation all are as maintained by the ITRS roadmap for sub-50nm gate length devices. The supplied voltage (V_{DD}) is given as 1V. ATLAS SILVACO TCAD is pressed into the service for the simulation of our prescribed device structure. Tonyplot is used for the structures and as well as output curve for the parameter extraction. Origin is further used for the plotting and comparing of response.

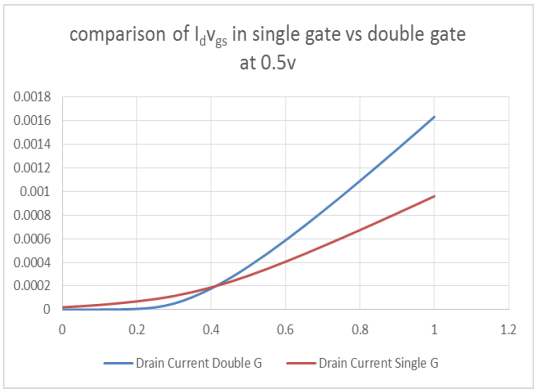
In an aspect of the ITRS roadmap, the drain bias voltage is fixed at V_{DD}=1.0V, same as to study the analog performances drain to source voltage V_{DS}=0.5V. The
Threshold voltages is obtained by $V_{TH}= V_{GS}-V_{GT}$, $I_{CONST}=10^{-16}$ A μ/m

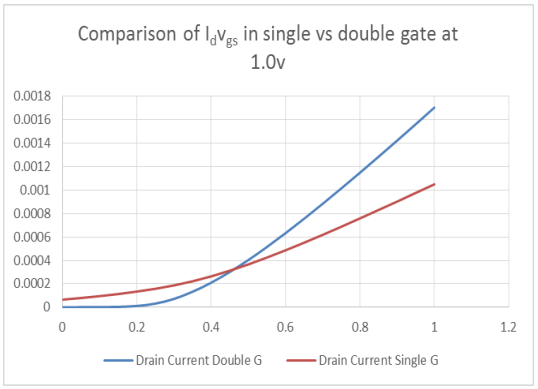
Models taken into account while simulation:

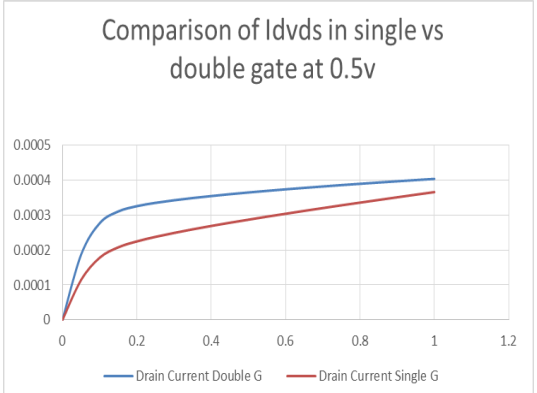
Name	Purpose
1) Inversion-layer Lombardi	To improve accuracy in the result of simulating constant voltage and temperature mobility
2) Fermi-Dirac uses rational Chebyshev approximation	To give result proximity to exact values
3)Auger Recombination Models	Basically used for minority carrier recombination
4) Gummel and Newton Techniques	Used calculations to obtain solutions
5) Read-Hall (SRH) Generation and Recombination	Simulating leakage currents arises due to the thermal generator

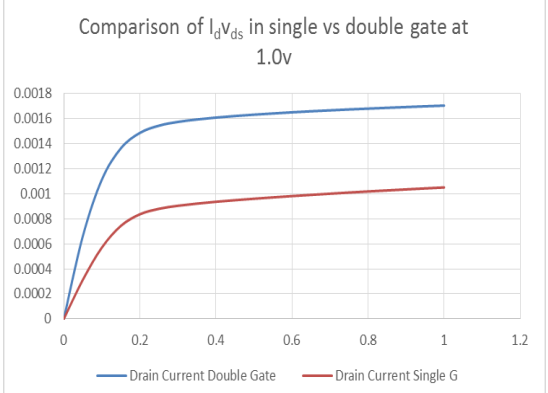
3. RESULT AND DISCUSSION

After simulation of both type of GATE devices, when we gave the different value at drain and gate, we obtain the series of drain current values. These values are thereby plotted and further compared side by side as shown in curves. The characteristics curve plotted below showing the comparison of I_dV_{gs} and I_dV_{ds} in SG MOSFET and DG MOSFET at 0.5v and 1.0v. The drain current depends upon the mobility of the carriers that is controlled by the doping concntrations.









The table below shows the comparative readings of the parameters which were further obtained after the simulation of single gate and double gate structures:-

GATE	THRESHOLD VOLTAGE (V_T) (V)	SUBTHRSHOLD SLOPE(SS) (mV decade^{-1})	I_{ON} (mV)	Transductance(gm_1) (S)	Output conductance(g_d) (S)
Single gate	**0.208691**	**58.1982**	**0.105106**	**0.0014831**	**0.00625702**
Double gate	**0.207896**	**77.1673**	**0.170521**	**0.00283179**	**0.00076118**

4. CONCLUSION

From the above simulation result of the structure of SG-MOSFET and DG-MOSFET (both SOI) we obtained values of the parameters, it can be seen that there is the influence of input given parameters on drain current obtained using the simulation software SILVACO. The operation of DG-MOSFET resulting in appreciable scalability, high current drive, low short channel effects, excellent transconductance.

With the use of high mobility channel materials in DG-MOSFET we can observe the lower short channel effects and lower leakage current.

From all this analysis we can see that DG-MOSFET have higher drain current drive than its counterpart SG-MOSFET. The DG-MOSFET is clearly observed to have better performance than SG-MOSFET in low power applications.

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