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Robust and reliable clock tree synthesis

Adarsh Mittal[1], Srishti Chadha[2]

[1]*Research Scholar, Nvidia Graphics Pvt Ltd, Bengaluru, Karnataka*

[2]*Research Scholar, IBM, Bengaluru, Karnataka*

ABSTRACT

The paper discusses various clock tree synthesis problems related to the robustness in sub-micron design nodes. The topic discussed include the clock polarity assignment problem for addressing the noise in power/ground, clock mesh design and synthesis problem for addressing the variation in clock delays and adjustable buffer delay assignment in order to support multi-voltage mode designs and parameters. The paper talks about the clock tree synthesis and the issues and difficulties faced because of the requirement of clock balancing. There are various parameters to improve the quality of the clock tree. It is important to have a reduced pessimism in the work optimization problems and the proposed techniques with regard to the circuit reliability in deep submicron design technology. The following subsections cover 1) the clock polarity assignment problem for reducing peak current noise on the clock tree. 2) The adjustable delay buffer (ADB) allocation and assignment problem that is useful in the multiple voltage modes design environment.

Keywords— *Clock tree improvement, Efficiency, Clock design, Clock tree constraints, Embedded systems and system on chip*

1. INTRODUCTION

In a synchronous computerized framework, the clock flag is utilized to characterize a period reference for the development of information in the framework. The clock dissemination organize circulates the clock signal(s) from a clock source to every consecutive component which requires it. Accordingly, the clockwork is essential to the activity of the synchronous framework. These days, significantly more consideration has been paid to clock related structure than at any other time. This is on the grounds that as the clock recurrence increments over a 1 GHz with low supply voltage, a little commotion on the clock flag causes a transient capacity mistake or even an extreme framework disappointment (the clamor originates from numerous components, for example, current charge/discharge variety and temperature variety). A standout amongst the most vital clock configuration issues is breaking down the clock signals and relieving the unfriendly effect of clock commotion on circuit unwavering quality.

This work reviews various imperative clock enhancement issues and the proposed strategies with respect to the circuit dependability in profound sub-micron structure innovation. The accompanying subsections cover 1) the clock extremity task issue for diminishing pinnacle current clamor on the clock tree, 2) the clockwork arrange structure issue for enduring the clock skew variety, 3) the customizable defer cushion (ADB) distribution and task issue that is helpful in the various voltage modes plan condition

2. CLOCK TREE SYNTHESIS

Usually, a clock tree synthesis (CTS) method consists of three important phases: the abstract tree topology generation, clock tree routing, and buffer/inverter insertion.

Fig. one shows the direction of flow of the ways of means that and medians (MMM) formula [1]. It accounts the clock sink locations as input associated generates an abstract clock tree topology by positioning the sinks in a recursion into two sub-regions till there is a unit at the most two sinks on every sub-areas. The partitions area unit performed either within the x-direction or in the y-direction, dividing the number of sinks equally applying the idea of the median. The partitions area unit then incorporated back in reverse order, which forms associate abstract tree topology wherever the merging points area unit determined by applying the concept of center of mass of the sink locations on the subregions to be incorporated. The additional correct determination of the placement of merging points (i.e., the inner nodes of the tree) is performed within the wire routing step.

With the theoretical topology acquired, the specific wire directing from the clock supply toward the sinks is accomplished by elective calculations. one among the preeminent eminent calculations is that the put off consolidation inserting (DME) algorithm [2], that guarantees zero clock skew though limiting the full clock wire length (the clock skew alludes to the defer refinement between the earliest point in time and most recent point so as to sinks). The DME algorithmic program keeps running in 2 phases; one might be a base up technique from sinks and furthermore, the following might be the best down strategy from the premise of the clock tree.

Figure 2 (a) and (b) demonstrate the base up the stage inside which the algorithmic program assembles combining fragments or consolidating locales if a delimited clock skew imperative is used. Each reason inside the combining area or locale fulfills the clock skew imperative for the time subtree nonmoving at the reason, accordingly the focuses inside the blending segment or region are the candidates for the wire spreading area of the internal node inside the dynamic tree

topology. Figure 2 (c) and 2 (d) illustrate the best downstage. The top-down stage finalizes the exact locations of branching positions. While all the points in merging area of the segments or regions satisfy the clock skew requirement constraint, depending on the location selection, the wire length may increase or decrease, and it is the top-down stage that ensures the minimal length of total wires.

The last advance of CTS is to add buffer into the clock tree. The clock slew-rate, which will be that the sharpness of the clock flag voltage rise and fall, ought to be controlled in stylish chip style. With huge clock trees, the wire capacitance is simply too enormous to ever be driven by one huge buffer put at the premise of the clock tree.

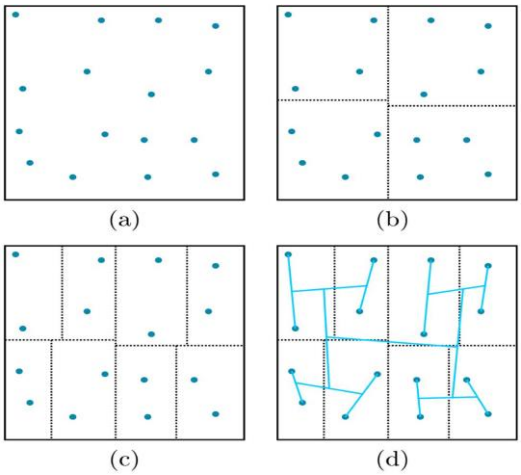

Fig. 1: The flow of the methods of means and medians algorithm

The location of all input clock sinks is fed as input. (b, c) Sinks are equally, using the concept of the median of sink locations, partitioned into subregions (arbitrarily in the x- or y-direction) until at most two sinks are left on each subregion. (d) The partitions are merged back in reverse order, using the concept of the mean (or center of mass) of the sink locations on the two regions.

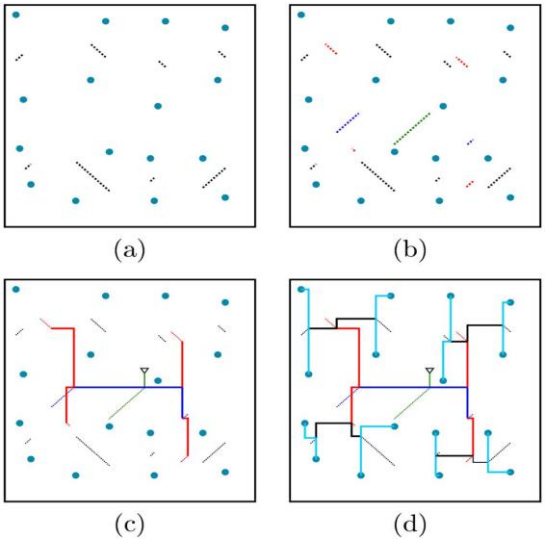

Fig. 2: The process of the deferred merge embedding algorithm

In above figure (a), (b) Merging segments, which are the candidates of points of clock tree branching locations, are constructed in a bottom-up manner. (c), (d) exact branching locations are identified and wire length minimization is performed in a top-down manner.

3. TECHNIQUES AND METHODOLOGIES

3.1 Clock polarity assignment

In synchronous circuits, clock trees and its timed burdens are the real wellsprings of on-chip commotion (control/ground voltage variances) since they switch at the same time close to the rising and additionally falling edge of the clock flag and draw a lot of current from the power/ground rail.

One approach to do as such is extra adaptability to this dispersing, by utilizing the extremity task method. It very well may be accomplished by blending cradles and inverters for clock buffering components that can scatter commotion over rising and falling edges of the check as appeared in Fig. 3. The methodology doled out a portion of the buffering components to a negative extremity and the other half positive by supplanting one of the two supports that are associated with the clock source with an inverter. Nonetheless, despite the fact that the aggregate pinnacle current is essentially lessened since power/ground commotion is a neighborhood impact, the issue remained to a great extent unsolved. Investigations have been done to blend cradles and inverters all through the clock tree structure so that for every neighborhood locale about a portion of the buffering components have positive extremity and the other half negative extremity. This methodology incredibly lessening clamor is probably going to present extensive clock skew. As per later information, blending supports and inverters for non-leaf components brought about a normal clock skew of more than 500 ps. This wonder is more conspicuous when the clock tree is certifiably not a parallel tree where one non-leaf buffering component has in excess of two leaf buffering components connected.

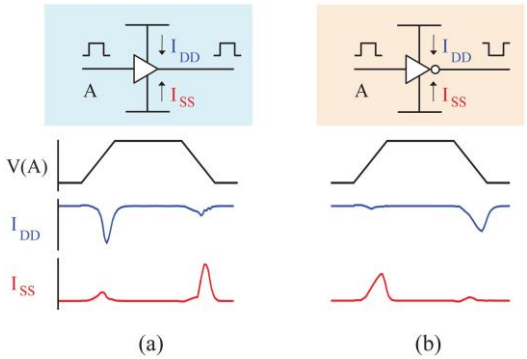

Fig. 3: Current profiles for a buffer and an inverter

3.2 Adjustable delay buffer allocation

Customary clock streamlining procedures are mostly founded on the earth in which all components in a circuit utilize one settled working voltage. In any case, an ongoing mechanical pattern requires different supply voltages to permit the voltage level connected to a circuit to be powerfully changed. In this multi-voltage mode structure, some piece of the circuit could work at high voltage when the related module is required to finish its preparing rapidly and at low voltage when timing necessity can be a loose and diminishing force is more vital. At the point when the provided voltage changes from high to low (or low to high), the postponement of all rationale components incorporating supports in the clock organize with respect to the chip likewise differs. One difficult issue in this multi-voltage mode configuration is the clock skew minor departure from the clock organizes.

To handle the clock skew variety issue, individuals have proposed a system of managing check skew enhancement in which they proposed utilizing ADB, which is an exceptionally structured support with the goal that its postponement can be

controlled powerfully. The general structure of ADB appears in figure 4. It is made out of a typical support, between capacitor bank, and a capacitor bank controller. The postponement of ADB could be balanced by actuating the inward capacitor bank. That is, the balanced deferral of ADB is dictated by the measure of actuated capacitors in the capacitor bank that is controlled by the capacitor bank controller and its control input.

Figure 5 exhibits how ADBs can be utilized to settle clock skew infringement. In Fig. 5a, an underlying clock tree with clock flag entry times for each check soak in two power modes is given. With the clock skew bound of 10, there is one clock skew infringement somewhere in the range of FF1 and FF6 in power mode 1. By supplanting cradle B1 with an ADB and embeddings an extra deferral of 3, this infringement can be settled. For power mode 2, there are two infringement, one somewhere in the range of FF3 and FF6 and the other somewhere in the range of FF2 and FF6. By apportioning ADBs at B1 and B3 and allotting their defer esteems with 4 and 1, individually, the clock skew infringement is evacuated. The subsequent ADB allotment appears in figure 5 (b).

The issue to be settled in utilizing ADBs in a multi-voltage mode configuration is to limit the expense of ADBs to be utilized since an ADB has a bigger number of transistors than a typical cradle because of the inward capacitor bank and controller.

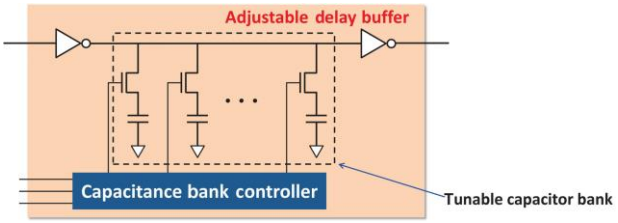

Fig. 4: Structure of adjustable delay buffer

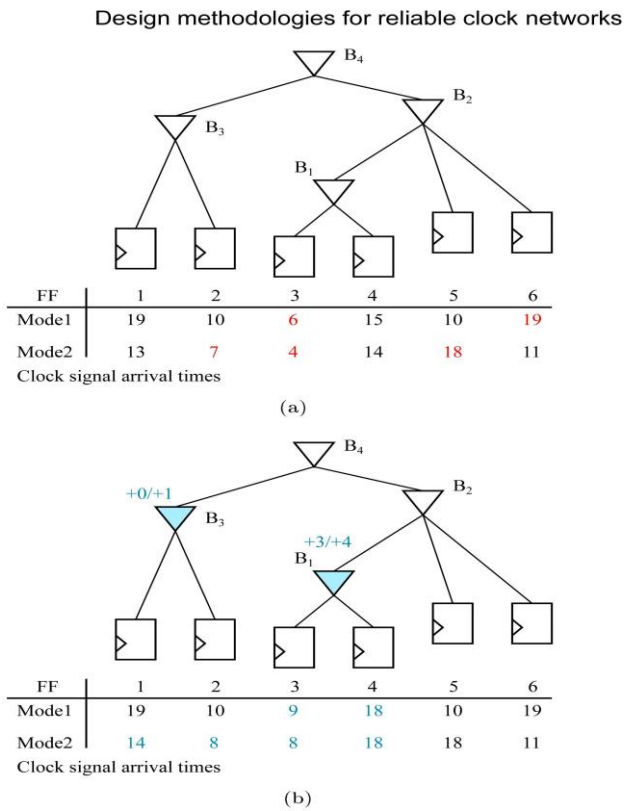

Fig. 5. An example clock tree with two power modes and the information of clock signal arrival times at clock sinks. (a) Underclock skew bound of 10, there exist clock skew violations. (b) Two adjustable delay buffers are allocated at B_1 and B_3 to resolve the violations.

4. CONCLUSION

As the procedure innovation downsizes, the variety or affect the ability of commotion and deferral in the clock arrange turns out to be more regrettable and more awful, which in truth causes an exceptional effect on the unwavering quality of the circuit. This paper investigated a few imperative clock related structure issues and the current procedures that are fundamental to the profoundly solid circuit plan. Notwithstanding the presented plan streamlining and amalgamation issues, there exist different issues that are additionally critical to endure or alleviate circuit commotion. Those models are 3D clock configuration considering through silicon by means of (TSV) structure variety and circuit dependability issues under the power-gated or clock-gated plan condition. We trust that this overview finds or evaluate for all intents and purposes valuable answers for the imperative clock advancement issues that emerge in the structures supporting assorted stages, applications or conditions.

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