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# Voltage Mode Universal Filter Using Current Conveyor

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**ABSTRACT**

*A second order voltage mode tunable universal filter is presented. The voltage mode filter is based on dual output second generation current controlled current conveyor (DOCCCII). The filter is capable of realizing high pass (HP), low pass (LP), band pass (BP), notch pass (NP) and all pass (AP) responses in voltage mode (VM). The filter employs only two capacitors and hence enjoys minimum component requirement. By properly exiting the filter structure with appropriate voltage signals the filter response in all four modes can be obtained. The filter enjoys tunability of quality factor and filter frequency. The filter is simulated in Hspice using 0.18µm CMOS model parameters obtained from TSMC. The DOCCCII works at a low supply voltage of ±1.5V.*

***Keywords: Current Mode; Current Conveyor; Universal Filter; Mix Mode.***

## 1. INTRODUCTION

Filters are an integral part of almost every electronic system and so their synthesis and development remain an ever evolving field. Among various filter structures, universal filters are the most versatile as all the standard filter functions can be derived from them [1]. They serve as a standalone solution to many filtering needs.

Owning to their inherent advantage of wide bandwidth, high slew rate, low power consumption, simple circuitry and excellent linearity [2-3] current conveyors (CC) are widely used in the electronic design. Moreover, the requirement of low voltage low power operation put forward by portable electronic devices and the energy harvesting systems [4-5] etc. further encourages the use of CC. The current controlled current conveyor (CCCII) is the most versatile active element due to its electronically tunable parasitic resistance [4, 6]. Numerous filter implementations utilizing CCCII can be found in the open literature [6]. The universal filter structure can be regarded as the most flexible as it can realize all the standard filter functions without any alteration in its topology.

In the past two decades, a number of voltage mode filters have been proposed utilizing different current mode active elements like dual output current controlled current conveyor (DOCCCII), multi output current conveyor (MOCCII) [6], current controlled current conveyor trans conductance amplifier (CCCCTA) [6], Current feedback operational amplifiers (CFOA) [6], fully differential current conveyor (FDCCII) [6], differential difference current conveyor and digitally programmable current conveyor (DPCCII)[6]etc. The literature survey shows that (i) they need more than two active elements [1, 7-8] (ii) they require three or more passive elements [1, 6-15]; (iii) Some of the filter response requires the component-matching conditions [9] (iv) Pole frequency cannot be tuned electronically [7, 9-15].

In this research paper, the authors propose a voltage mode universal filter designed by two DOCCCII. The filter uses only two capacitors for the design. By proper excitation, with appropriate voltage signals, the filter structure can work as a universal filter. The filter is capable of realizing high pass (HP), low pass (LP), band pass (BP), notch pass (NP) and all pass (AP) responses in voltage mode. The pole frequency of the filter is tunable by changing the bias current of the CCCII. The filter works at a low supply voltage of ±1.5V.

 

## 2. DUAL OUTPUT CURRENT CONTROLLED CURRENT CONVEYOR (CCCII)

The concept of the CCCII is similar to that of CCII with an exception that it has a tunable parasitic resistance at the X terminal which is tunable via bias current. This makes CCCII superior in design than CCII since it requires no external resistance for activation [4]. The V-I relationship of the CCCII is presented in the matrix (1) and the block diagram is shown in Fig. 1.

$$\begin{bmatrix} V_X \\ I_Y \\ I_Z \end{bmatrix} \begin{bmatrix} R_X & 1 & 0 \\ 0 & 0 & 0 \\ \pm 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ V_Z \end{bmatrix} \qquad (1)$$

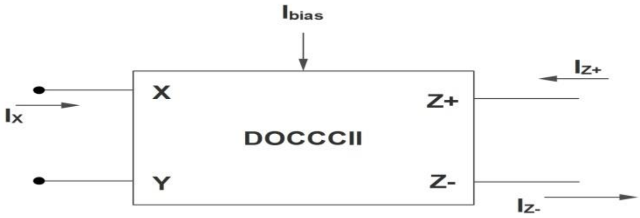


**Fig. 1: Block diagram of DOCCCII**

The CMOS implementation of a class AB DOCCCII is presented in Fig. 2. The circuit consists of a translinear loop (transistors M1 – M4). Two current mirrors (transistors M5 – M6 and M7 – M8) are used to bias the translinear loop with bias current $I_b$, the input cell presents a high impedance at voltage input node Y and a low input impedance at current input node X. This cell acts as a voltage follower. The current at node X is copied to output nodes Z+ and Z–. The cross coupled current mirrors are used to generate negative current at Z- node. The parasitic resistance at the X node can be evaluated using the equations (2-3).

$$R_X = \frac{1}{g_{m2} + g_{m4}} \qquad (2)$$

$$g_{mi} = \sqrt{2\beta_n I_B} \qquad \text{(n=2,4)} \qquad (3)$$

Where $\beta_n = \mu_n C_{ox} \frac{W}{L}$ is the physical parameter of the MOS transistor and $g_{m2}$ & $g_{m4}$ are the trans conductance of the transistors M2 and M4 respectively which are controllable through bias current $I_B$.

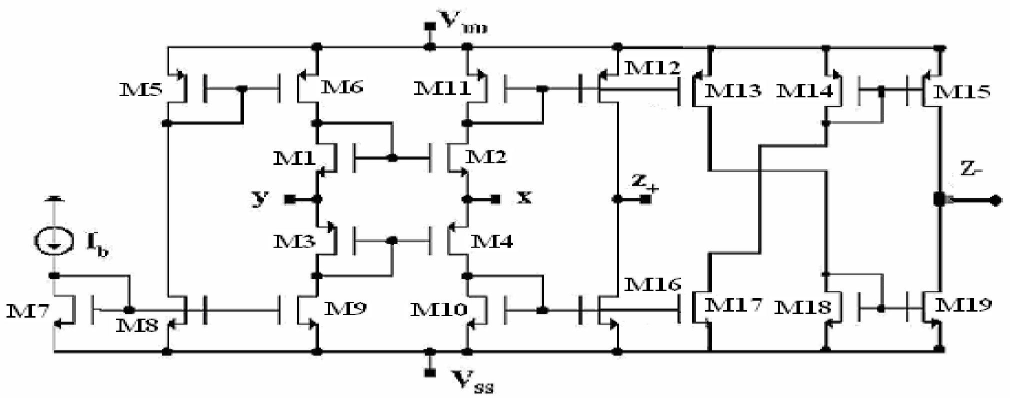


**Fig. 2: CMOS implementation of DOCCCII**

## 3. THE PROPOSED MIXED MODE FILTER

The proposed voltage mode MISO type universal filter consists of only two DOCCCII, two capacitors as presented in Fig. 3. The filter is capable of realizing all five generic filter functions in VM operation. The proposed filter structure does not require any passive resistors thus making it a minimum component resistor less implementation.

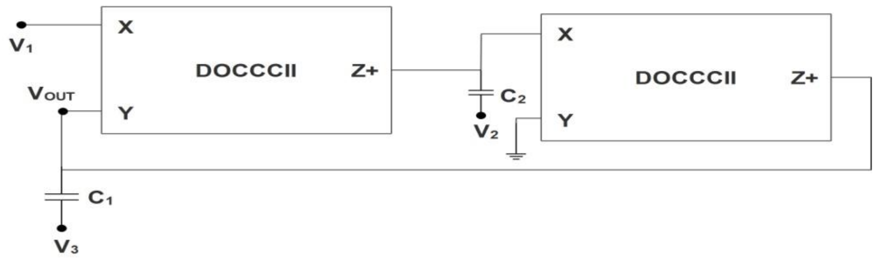


**Fig. 3: Proposed Voltage Mode Universal Filter**

The routine analysis of the filter leads to the transfer function as given in equation 4. In voltage mode operation a combination of three input voltages is required. The output is obtained from $V_{Out\ 1}$ the node.

$$V_{Out\ 1} = \frac{V_3(S^2C_1C_2R_{x1}R_{x2}+SC_1R_{x1})+V_1-V_2SC_2R_{x1}}{S^2C_1C_2R_{x1}R_{x2}+SC_1R_{x1}+1} \quad (4)$$

From (4) it can be deduced that by properly selecting input voltages $V_1$, $V_2$ and $V_3$ all the responses can be obtained. The input sequence to be applied is given in Table 1. For realizing AP function $V_2$ must be twice of the other two input voltages.

**Table 1:** Input sequence for voltage mode operation

| Output | Inputs | | |
|---|---|---|---|
| $V_{Out}$ | $V_1$ | $V_2$ | $V_3$ |
| LP | 1 | 0 | 0 |
| HP | 0 | 1 | 1 |
| BP | 0 | 1 | 0 |
| NP | 1 | 1 | 1 |
| AP | 1 | 2 | 1 |

The quality factor $Q$, natural frequency $\omega_o$ and bandwidth of the filter are given in equations (5-7). It can be inferred from the expressions that by changing the bias currents while keeping their ratio constant. The $Q$ and $\omega_o$ of the filter can be tuned independently.

$$Q_O = \sqrt{\frac{C_2R_{x2}}{C_1R_{x1}}} \quad (5)$$

$$\omega_O = \sqrt{\frac{1}{C_2R_{x2}C_1R_{x1}}} \quad (6)$$

$$BW = \frac{\omega_O}{Q_O} = \frac{1}{c_2R_{x2}} \quad (7)$$

**4. SIMULATION RESULTS**

To establish the workability of the proposed filter structure it was examined using H-Spice. The design of the DOCCCII is critical as it dictates the characteristics of the designed filter. In this research, the DOCCCII is designed in 0.18µm TSMC technology. The aspect ratios of the transistors are given in Table 2. The main parameters of the DOCCCII are the voltage transfer gain β(s) and current transfer gain ±α(s) and their frequency behaviors. The important parameters of the DOCCCII are measured for the bias current of 20uA.

**Table 2:** Aspect ratios of the transistors

| Transistors | W(µm) | L(µm) |
|---|---|---|
| M1, M2 | 30 | 0.18 |
| M3, M4 | 90 | 0.18 |
| M5 | 45 | 2 |
| M6 | 50 | 2 |
| M7, M8, M9, M10 | 15 | 2 |
| M11, M12, M13, | 45 | 1 |
| M18, M19 | 20 | 1 |
| M14, M15 | 60 | 1 |
| M16, M17 | 15 | 1 |

The frequency response of the current and voltage transfer gain is shown in Fig. (4-5) for different bias currents. The voltage transfer bandwidth is obtained by giving input at Y node and measuring the output at X node which is terminated by a very high resistance. The Z terminals are grounded. The current transfer bandwidth is obtained by applying input current at X node and measuring the output current at Z node. The Y node is grounded in this case.

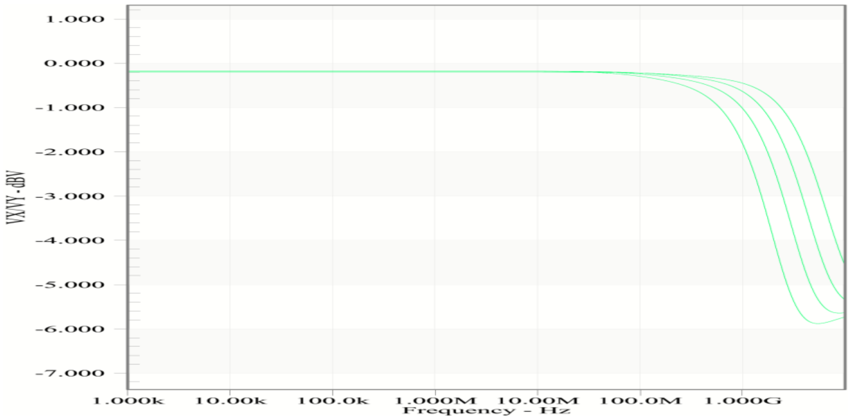


**Fig. 4: The voltage transfer bandwidth of DOCCCII for different bias currents**

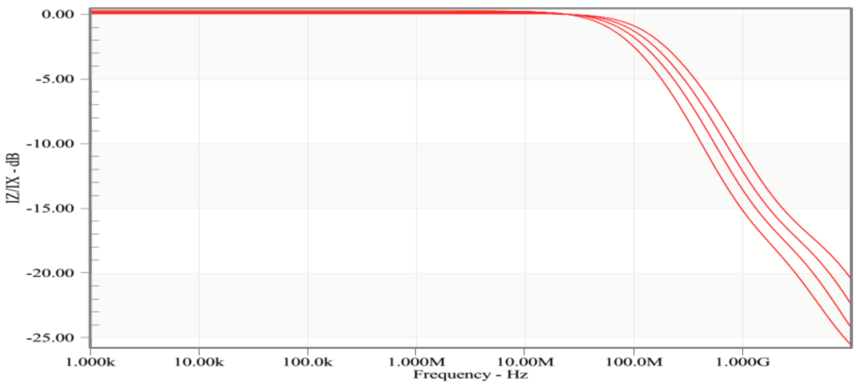


**Fig. 5: The current transfer bandwidth at Z+ node of DOCCCII for different bias currents**

The proposed voltage mode filter is tested at a bias current of 20µA. The values of the capacitors are set at $C_1$=$C_2$=250pF. The parasitic resistances $R_{x1}$ and $R_{x2}$ of the two DOCCCII are 796.063Ω for the specified bias current. The universal filter structure is simulated to validate the VM operation. The Fig. 6 presents the responses for the VM filter. The Fig. 7 gives the phase response of the VM all pass filter.

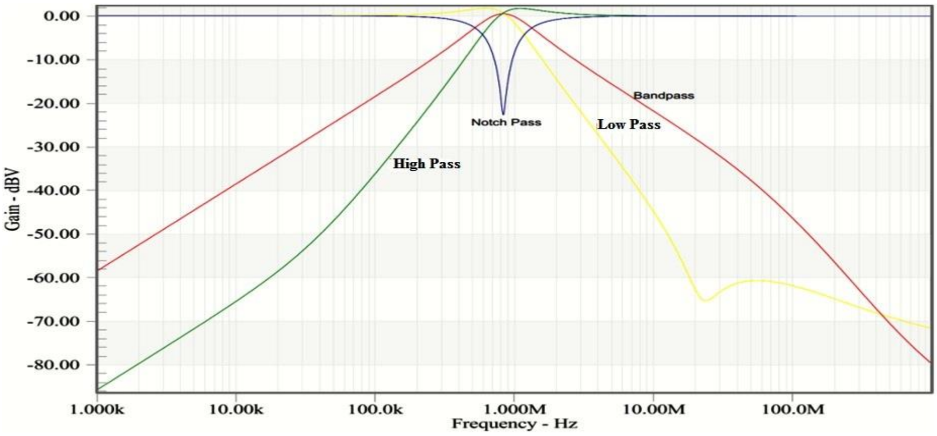


**Fig. 6: Voltage mode response of the mixed mode universal filter**

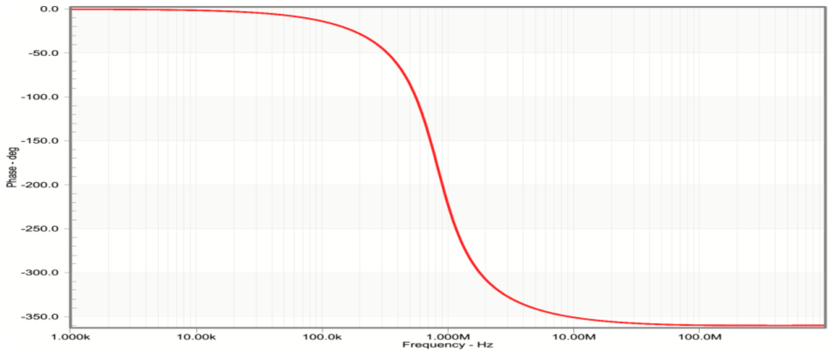


**Fig. 7: Phase of the all pass voltage mode filter**

The time domain analysis was also performed. A sinusoidal signal of 800mV p-p is applied at a frequency of 10MHz and the HP response of the VM filter is noted as given in Fig. 8. The analysis reveals that the filter operates with minimum distortion and hence suitable for signal processing.

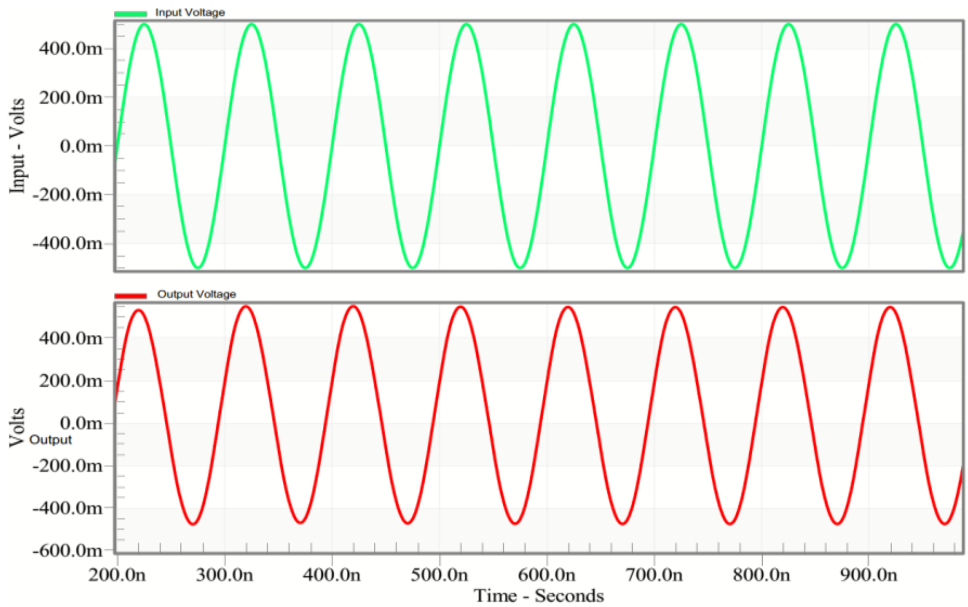


**Fig. 8: Time domain analysis of the HP output of the voltage mode filter**

  

**5. CONCLUSION**

In this paper a second order voltage mode universal filter is proposed. The filter can perform in voltage mode. The filter enjoys requirement of minimum components only two DOCCCII and two capacitors. The utilization of DOCCCII removed the requirement of external resistors. By proper excitation the filter is capable of realizing HP, LP, BP, NP and AP response in Voltage mode. The filter frequency and quality factor can be independently tuned via bias current.

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